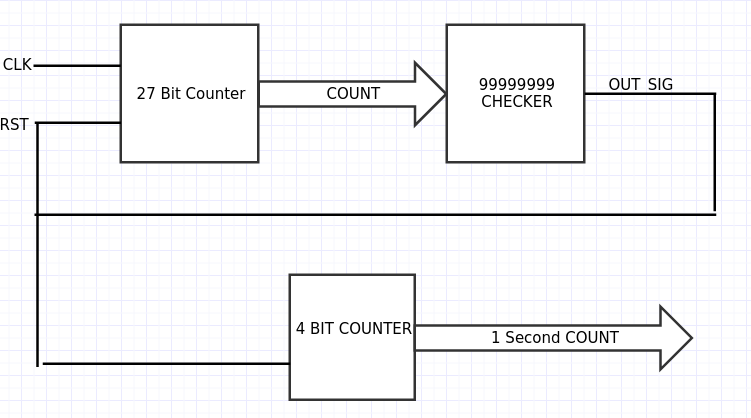
**Clock Divider**

**1.**



**2.** The goal of this task was to create a 4 bit counter that incremented every second. To do this, we had to implement two counters in the same fashion described above. What was different was that one of the counters had to count to 100 MHz (this is the frequency at which the clock ran). We had the first counter count from 0 to 99,999,999 and on it’s terminal count, we incremented the second clock. Therefore, every 100 M clock pulses, or every second, we incremented the secondary counter having it count up every second.

**3.**

===

\*.v

===

`timescale 1ns / 1ps

`define N\_BIT 27

`define DIVIDE 99999999

module clock\_divider\_2(clk,rst,LED);

//input outputs

input wire clk;

input wire rst;

output reg [3:0] LED;

//internal wirings

reg [`N\_BIT-1:0] in\_cnt;

wire trig;

assign trig = (in\_cnt == `DIVIDE);

//main clk to initialize and count inner count

always@(posedge clk, posedge rst)

begin

if (rst | trig)

begin

in\_cnt <= `N\_BIT'b0;

end

else

in\_cnt <= in\_cnt + 1'b1;

end

always @(posedge trig, posedge rst)

begin

if (rst)

LED <= 4'b0000;

else

begin

LED <= LED + 1'b1;

end

end

endmodule

====

\*TB.v

====

`timescale 1ns / 1ps

module clock\_divider2\_TB;

// Inputs

reg clk;

reg rst;

// Outputs

wire [3:0] LED;

// Instantiate the Unit Under Test (UUT)

clock\_divider\_2 uut (

.clk(clk),

.rst(rst),

.LED(LED)

);

initial begin

// Initialize Inputs

clk = 0;

rst = 1;

#2 rst = 0;

// Wait 100 ns for global reset to finish

#10000 $finish;

// Add stimulus here

end

always

#1 clk = ~clk;

endmodule

====

\*.ucf

====

## Clock signal

NET "clk" LOC = "V10" | IOSTANDARD = "LVCMOS33"; #Bank = 2, pin name = IO\_L30N\_GCLK0\_USERCCLK, Sch name = GCLK

Net "clk" TNM\_NET = sys\_clk\_pin;

TIMESPEC TS\_sys\_clk\_pin = PERIOD sys\_clk\_pin 100000 kHz;

## Leds

NET "LED<0>" LOC = "U16" | IOSTANDARD = "LVCMOS33"; #Bank = 2, Pin name = IO\_L2P\_CMPCLK, Sch name = LD0

NET "LED<1>" LOC = "V16" | IOSTANDARD = "LVCMOS33"; #Bank = 2, Pin name = IO\_L2N\_CMPMOSI, Sch name = LD1

NET "LED<2>" LOC = "U15" | IOSTANDARD = "LVCMOS33"; #Bank = 2, Pin name = IO\_L5P, Sch name = LD2

NET "LED<3>" LOC = "V15" | IOSTANDARD = "LVCMOS33"; #Bank = 2, Pin name = IO\_L5N, Sch name = LD3

## Buttons

NET "rst" LOC = "B8" | IOSTANDARD = "LVCMOS33"; #Bank = 0, Pin name = IO\_L33P, Sch name = BTNS

**4.**

========================

Advanced HDL Synthesis Report

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Macro Statistics

# Counters : 2

27-bit up counter : 1

4-bit up counter : 1

# Registers : 31

Flip-Flops : 31

Top Level Output File Name : clock\_divider\_2.ngc

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\* Design Summary \*

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Primitive and Black Box Usage:

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# BELS : 124

# GND : 1

# INV : 2

# LUT1 : 26

# LUT2 : 1

# LUT3 : 3

# LUT4 : 1

# LUT5 : 1

# LUT6 : 35

# MUXCY : 26

# VCC : 1

# XORCY : 27

# FlipFlops/Latches : 31

# FDC : 31

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 5

# IBUF : 1

# OBUF : 4

Device utilization summary:

---------------------------

Selected Device : 6slx16csg324-3

Slice Logic Utilization:

Number of Slice Registers: 31 out of 18224 0%

Number of Slice LUTs: 69 out of 9112 0%

Number used as Logic: 69 out of 9112 0%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 69

Number with an unused Flip Flop: 38 out of 69 55%

Number with an unused LUT: 0 out of 69 0%

Number of fully used LUT-FF pairs: 31 out of 69 44%

Number of unique control sets: 2

IO Utilization:

Number of IOs: 6

Number of bonded IOBs: 6 out of 232 2%

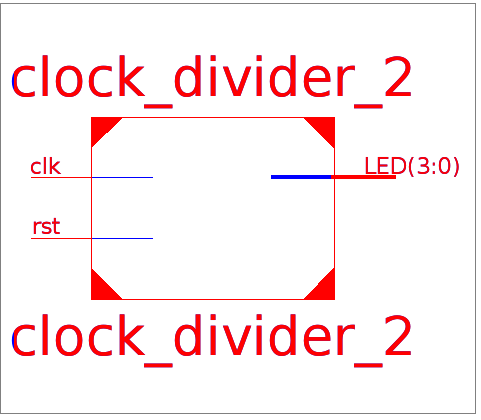
Specific Feature Utilization:

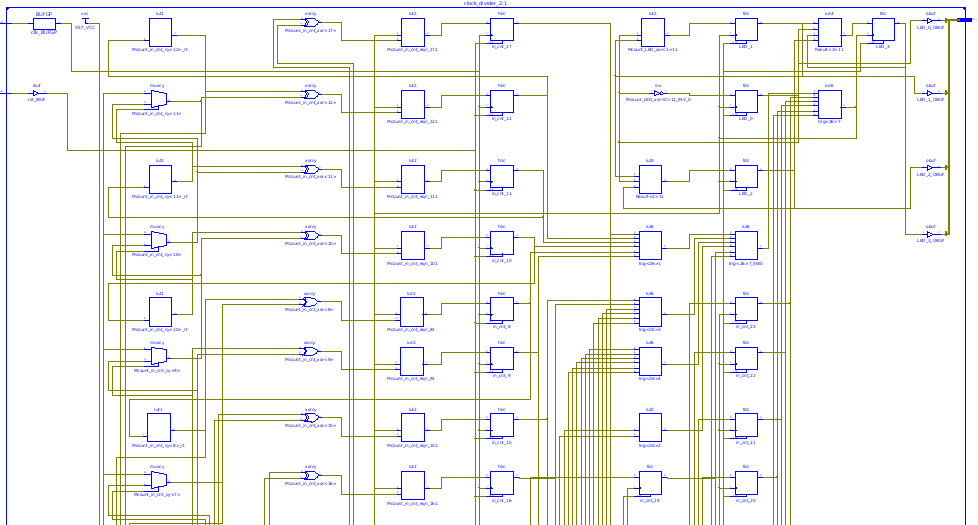
Number of BUFG/BUFGCTRLs: 1 out of 16 6%

**5. Device Utilization Summary**

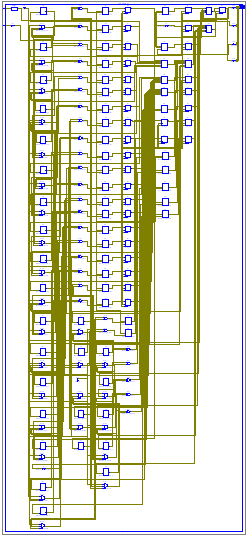
|  |  |  |  |
| --- | --- | --- | --- |
| Slice Logic Utilization | Used | Available | Utilization |
| # of Slice Registers | 31 | 18,224 | 1% |
| # used as Flip Flops | 31 |  |  |
| # of Slice LUTs | 68 | 9,112 | 1% |
| # used as logic | 67 | 9,112 | 1% |
| # using O6 output only | 40 |  |  |
| # using O5 output only | 25 |  |  |
| # using O5 and O6 | 2 |  |  |
| # used as route-thrus only | 1 |  |  |
| # of occupied Slices | 20 | 2,278 | 1% |
| # of MUXCYs used | 28 | 4,556 | 1% |
| # of LUT Flip Flop pairs used | 68 |  |  |
| # with an unused Flip Flop | 38 | 68 | 55% |
| # of fully used LUT-FF pair | 30 | 68 | 44% |
| # of unique control sets | 2 |  |  |
| # of slice register sites lost to control set restrictions | 9 | 18,224 | 1% |
| # of bonded IOBs | 6 | 232 | 2% |
| # of BUFG/BUFGMUXs | 1 | 16 | 6% |
| # used as BUFGs | 1 |  |  |
| Average Fanout of Non-Clock Nets | 3.91 |  |  |

**6. High Level Schematic**





\*\*Closer view of below



**7. Maximum Frequency:** 344.947MHz

**8. Waveform**

